SSSTC

Solid State Storage Technology Corporation (**KIOXIA** Group)

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ENGINEERING SPECIFICATIONS

Product Name: CL6 Series

Solid State Drives
GENERIC

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Solid State Storage Technology Corporation (**KIOXIA** Group)

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Version	History	Date
1.0	First Release	2023/07/14
1.1	Modify MTBF	2023/07/19
1.2	Add Models for Extended and Industrial Temperature Range	2024/03/01

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Safety Precautions

This section lists important precautions which users of our product(s) (and anyone else) should observe in order to avoid injury to human body and damage to property, and to ensure safe and correct use of our products. Please be sure that you understand the meanings of the labels and graphic symbols described below before you move on to the detailed descriptions of the precautions, and comply with the precautions stated.

Explanation of Labels

⚠DANGER	⚠WARNING	⚠CAUTION	*NOTICE*
Indicates a hazardous situation which, if not avoided, will result in death or serious injury[1].	Indicates a hazardous situation which, if not avoided, could result in death or serious injury[1].	Indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury[2].	Indicates practices that may cause property damage[3] and other problems, but not personal injury

[1]Serious injury includes blindness, wounds, burns (low and high temperature), electric shock, fractures, and poisoning, etc. with long-lasting effects or that require hospitalization and/or long-term hospital visits for treatment.

[2]Minor or moderate injury includes wounds, burns, electric shock, etc. not requiring hospitalization and/or long-term hospital visits for treatment.

[3]Property damage means damage to customer or third-party machines and equipment.

Explanation of Graphic Symbols

 **Prohibited**	 **Instructions**
Indicates prohibited actions.	Indicates actions that must be undertaken for safety purposes.

LIMITATION OF LIABILITY

Solid Corporation and its subsidiaries and affiliates are collectively referred to as "SSSTC".

- SSSTC shall not be liable for any damage due to the fault or negligence of users, fire, earthquake, or other accident beyond the control of SSSTC.
- SSSTC shall not be liable for any incidental or consequential damages including but not limited to change or loss of stored data, loss of profit, or interruption of business, which are caused by use or non-usability of the product.
- SSSTC shall not be liable for any damage result from failure to comply with the contents in the product specification.
- SSSTC shall not be liable for any damage based on use of the product in combination with connection devices, software, or other devices provided by SSSTC with the product.

SAFETY

⚠CAUTION	
Prohibited	Do not drop. *Dropping the drive may cause injury or damage to the drive.*
Prohibited	Do not touch sharp edges or pins of the drive. *Sharp edges and protrusions etc. may cause injury. Hold the drive by both sides when carrying it.*
Prohibited	Do not remove any labels from the drive or deface them in any way. Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy the drive, whether in whole or in part. *Failure to do so voids any warranty, expressed or implied, and may cause injury, failure, or data loss.*
Prohibited	Do not subject the drive to extreme shock such as dropping, upsetting, or crashing against other objects. *Extreme shock to the drive may cause damage to it, data corruption, etc.*
Prohibited	Do not stack the drive on another drive or on other parts etc. or stack another drive or other parts etc. on the drive during storage or transportation. *Shock, stress or weight may cause parts distortion etc.*
Prohibited	Avoid attachment of these materials. *Attachment of conductive and/or dielectric materials such as metal powder, liquid, etc. to live parts such as printed circuit board patterns or pins etc. may cause damage to the drive.*
Prohibited	Do not subject the semiconductor parts on board to external extreme stress and/or pressure. *Semiconductor parts on board may be damaged by external extreme stress and/or pressure.*
Prohibited	High temperature. Do NOT touch the drive while it is hot to prevent skin burns upon contact. *Electronic components become hot during operation. Allow all components to cool down after disconnecting power before contact.* 

⚠CAUTION	
 **Instructions**	Follow the specifications for Chapter “POWER REQUIREMENTS”, Chapter “ENVIRONMENTAL LIMITS”, etc. when using. *Failure to do so may cause damage to the drive.*
 **Instructions**	Follow Section “Required power-off sequence” when you turn off power supply. *If the power to the drive is lost during drive operation, the data in the write cache will be lost.*
 **Instructions**	To protect against accidental data loss, back up your data frequently on multiple types of storage media. *There is a certain probability of the drive causing failure including data error or data loss.* *(Request) Please include this in the instruction manual etc. of the system in which this device is used and ensure that users are made thoroughly aware of it.*
 **Instructions**	Take anti-static measures to avoid damage to the drive when handling. *The drive uses parts susceptible to damage due to ESD (electrostatic discharge).* *Always ground yourself with such as ESD proof wrist strap connected to ground before handling.*
 **Instructions**	Exchange the drive after the power of the drive turned off, except using the hot-pluggable drive and the system, which meets the requirements for hot plug. *Inserting or pulling out the drive while power is supplied may cause damage to the drive.*

Table of Contents

1 INTRODUCTION

1.1 Overview:

The CL6 series Solid State Drive (SSD) delivers leading performance in an industry standard PCIe M.2 form factor while simultaneously improving system responsiveness for applications over standard rotating drive media or hard disk drives. By combining leading NAND flash memory technology with our innovative high performance firmware, ***Solid State Storage Technology Corporation*** delivers a SSD for PCIe hard disk drive drop-in replacement with enhanced performance, reliability, ruggedness and power savings. Since there are no rotating platters, moving heads, fragile actuators, or unnecessary delays due to spin-up time or positional seek time that can slow down the storage subsystem, significant I/O and throughput performance improvement is achieved as compared to rotating media or hard disk drives. This document describes the specifications of the CL6 series SSD in M.2 form factors.

The C6 series M.2 SSD primarily targets M.2 based laptop PCs, highly rugged client devices, as well as thin and light mini/sub-notebooks. Key attributes include high performance, low power, increased system responsiveness, high reliability, and enhanced ruggedness as compared to standard hard drives. The CL6 series M.2 SSD is available in the form factors and capacities listed in Table 1-1 that are electrically, mechanically, and software compatible with existing M.2 slots. Our flexible design allows interchangeability with existing hard drives based on the M.2 interface standard

1.2 Product Specification

1.2.1. Form Factor & Capacity:

Table 1-1 Product number, Capacity and Form Factor

Class	Model Name	Capacity	Form Factor
Standard	CL6-3D256	256 GB	M.2 Type 2230-S2-M
	CL6-3D512	512 GB	
	CL6-3D1024	1024 GB	
	CL6-3D2048	2048 GB	M.2 Type 2230-S3-M
	CL6-4D256	256 GB	M.2 Type 2242-S2-M
	CL6-4D512	512 GB	
	CL6-4D1024	1024 GB	
	CL6-4D2048	2048 GB	M.2 Type 2242-S3-M
	CL6-8D256	256 GB	M.2 Type 2280-S2-M
	CL6-8D512	512 GB	
	CL6-8D1024	1024 GB	
	CL6-8D2048	2048 GB	M.2 Type 2280-S3-M
Extended	CL6-3U256	256 GB	M.2 Type 2230-S2-M
	CL6-3U512	512 GB	
	CL6-3U1024	1024 GB	
	CL6-3U2048	2048 GB	M.2 Type 2230-S3-M
	CL6-4U256	256 GB	M.2 Type 2242-S2-M
	CL6-4U512	512 GB	
	CL6-4U1024	1024 GB	
	CL6-4U2048	2048 GB	M.2 Type 2242-S3-M
	CL6-8U256	256 GB	M.2 Type 2280-S2-M
	CL6-8U512	512 GB	
	CL6-8U1024	1024 GB	
	CL6-8U2048	2048 GB	M.2 Type 2280-S3-M
Industrial	CL6-3V256	256 GB	M.2 Type 2230-S2-M
	CL6-3V512	512 GB	
	CL6-3V1024	1024 GB	
	CL6-3V2048	2048 GB	M.2 Type 2230-S3-M
	CL6-4V256	256 GB	M.2 Type 2242-S2-M
	CL6-4V512	512 GB	
	CL6-4V1024	1024 GB	
	CL6-4V2048	2048 GB	M.2 Type 2242-S3-M
	CL6-8V256	256 GB	M.2 Type 2280-S2-M
	CL6-8V512	512 GB	
	CL6-8V1024	1024 GB	
	CL6-8V2048	2048 GB	M.2 Type 2280-S3-M

1.2.2. User Addressable Sectors:

Table 2 User Addressable Sectors

Unformatted capacity	Total user addressable sectors in LBA mode
256GB	500,118,192
512GB	1,000,215,216
1024GB	2,000,409,264
2048GB	4,000,797,360

Notes:

1). 1GB=1,000,000,000 bytes and not all of the memory can be used for storage.

2). 1 Sector = 512 bytes

1.2.3. Flash:

Triple-Level Cell (TLC) component with Toggle-Mode

1.2.4. Band Performance

Table 3 Maximum Sustained Read and Write Bandwidth on Windows 10 platform

Capacity	Access Type	MB/s (typ.)
256 GB	Sequential Read	4400
	Sequential Write	3000
512 GB	Sequential Read	4800
	Sequential Write	4000
1024 GB	Sequential Read	6000
	Sequential Write	5000
2048 GB	Sequential Read	6000
	Sequential Write	5300

Notes:

1). Performance measured using CrystalDiskMark 8.0.4b, 1MiB QD8 T1, 1GiB test size, 5 cycles.

2). PCIe link speed is Gen4 x 4.

3). Write cache enabled & 4K boundary data.

4). Test by secondary drive (data drive & clean state).

5). Performance based on internal testing on ROG STRIX Z690-E Gaming / 12th Gen Intel(R) Core(TM) i7-12700K 3.60 GHz, Windows 10; Performance may vary on different platforms, NVMe driver and OS.

6). These values which are written as “typ.” are the values obtained in specific test environment at SSSTC and for reference purpose only. SSSTC does not warrant those values.

1.2.5. Read and Write IOPS

Table 4 Random Read/Write Input/Output Operations per Second on Windows 10 platform

Capacity	Access Type	IOPS(typ.)
256 GB	4K Read (IOPS)	350K
	4K Write (IOPS)	700K
512 GB	4K Read (IOPS)	650K
	4K Write (IOPS)	850K
1024 GB	4K Read (IOPS)	650K
	4K Write (IOPS)	900K
2048 GB	4K Read (IOPS)	900K
	4K Write (IOPS)	900K

Notes:

1). Performance measured using CrystalDiskMark 8.0.4b, 4KiB QD32 T16, 1GiB test size, 5 cycles.

2). PCIe link speed is Gen4 x 4.

3). Write cache enabled & 4K boundary data.

4). Test by secondary drive (data drive & clean state).

5). Performance based on internal testing on ROG STRIX Z690-E Gaming / 12th Gen Intel(R) Core(TM) i7-12700K 3.60 GHz, Windows 10; Performance may vary on different platforms, NVMe driver and OS.

6). These values which are written as “typ.” are the values obtained in specific test environment at SSSTC and for reference purpose only. SSSTC does not warrant those values.

1.2.6. Ready Time

Table 5 Power on to Ready time Specifications

Power-on Sequence	Typical POR	Sudden POR
Complete the I/O Command	500ms	10s

Notes:

1). Write cache enabled

2). Device measured using Drive Master

3). PCIe link speed is Gen4 x 4.

4). Test results may be different on different platform.

5). Typical POR assumes proper shutdown (Power removal preceded by host Shutdown Notification)

1.2.7. Compatibility

-- NVM Express Specification

-- PCI Express Base Specification

-- PCI Express M.2 Electromechanical Specification

-- Microsoft latest WHCK Certification

-- Support Legacy and UEFI BIOS

-- Security

Non-SED model (Pyrite)

- NVMe Security Send and Security Receive commands are supported
- TCG Storage Security Subsystem Class: TCG Pyrite Version 2.01 is supported 2)
- Storage Interface Interactions Specification (SIIS) Version 1.10 is supported 2)
- Firmware is protected by Digital signature (RSASSA_PKCS_v1_5(RSA3072,SHA384))

SED model

- NVMe Security Send and Security Receive commands are supported
- TCG Storage Security Subsystem Class: TCG Opal Version 2.01 is supported 2)
- TCG Storage Interface Interactions Specification(SIIS) Version 1.10 is supported 2)
- XTS-AES 256 is supported 2)
- TCG Storage Feature Set: Block SID Authentication is supported 2)
- Firmware is protected by Digital signature (RSASSA_PKCS_v1_5(RSA3072,SHA384))

1.2.8. Supported Operating System and Chipset

--Operating System

Windows 7 x86, x64 / Windows 8 x86, x64 / Windows 10

Linux series, Red Hat 6.5, Fedora, SUSE, Ubuntu

Windows Server 2008, 2012

--Chipset:

※Please make sure the BIOS of the used mother board be updated to the latest version.

Table 5 Tested platform w/o issues

Manufacturer	Platform	Chipset	Manufacturer	Platform	Chipset
Echo 13	Alienware AW13R2	Intel Sunrise Point-LP	Precision	7440 AIO	Intel Sunrise Point Q170
Echo 15	Alienware AW15R2	Intel Sunrise Point HM170	Precision	3420 SFF	Intel Sunrise Point C236
Echo 17	Alienware AW17R3	Intel Sunrise Point HM170	Precision	3620MT	Intel Sunrise Point C236
XPS 13	9350	Intel Sunrise Point-LP	Optiplex	3040 MT	Intel Sunrise Point H110
Precision	5510	Intel Sunrise Point CM236	Optiplex	3240 AIO	Intel Sunrise Point H110
XPS 15	9550	Intel Sunrise Point HM170	ASUS	Z170 DELUXE	Intel Sunrise Point Z170
Inspiron 15	7568	Intel Sunrise Point-LP			
Optiplex	3040 MT	Intel Sunrise Point H110			
OptiPlex	3240 AIO	Intel Sunrise Point M110			
ProDesk	490 G3 MT	Intel Sunrise Point H170			
ProDesk	600 G2 DM	Intel Sunrise Point Q150			
Inspiron	5559	Intel Sunrise Point-LP			
Inspiron 11	3153	Intel Sunrise Point-LP			
Inspiron 13	7353	Intel Sunrise Point-LP			
Predator 15	G9-591	Intel Sunrise Point HM170			
MS	Surface Pro 4	Intel Sunrise Point-LP			
XPS Desktop	8900	Intel Sunrise Point Z170			
Alienware	X51 R3	Intel Sunrise Point Z170			
OptiPlex	7040 SFF	Intel Sunrise Point Q170			
OptiPlex	5040 SFF				

1.2.9. Certifications

Table 7 Device Certifications

Certification	Description
CE compliant	Indicates conformity with the essential health and safety requirements set out in European Directives Low voltage Directive and EMC Directive
UL certified	Underwriters Laboratories, Inc. Component Recognition UL60950-1
BSMI	Compliance to the Taiwan EMC standard "Limits and methods of Radio Disturbance Characteristics of Information Technology Equipment, CNS 13438 Class B"
Microsoft WHQL	Microsoft Windows Hardware Quality Labs
RoHS compliant	Restriction of Hazardous Substance Directive

1.2.10. PCIe M.2 interface Power Management

3.3V Input/ Max current (Peak) : 1.8

1.2.11. Power Consumption

Table 8 Operating Voltage & Current

Description	Min	Max	Unit
Operating voltage for 3.3V (+/- 8%)	3.036	3.564	V

Table 9 Power Consumption

Capacity	Operation (Ta = 25°C)	Typical[1)]	Max (RMS T=5s)	Unit
256GB	Read[2)]	4.3	4.8	W
	Write[2)]	3.7	4.7	W
	PS3[3)]	20	-	mW
	PS4[3)]	3	-	mW
512GB	Read[2)]	4.7	5.7	W
	Write[2)]	4.2	5.3	W
	PS3[3)]	20	-	mW
	PS4[3)]	3	-	mW
1024GB	Read[2)]	4.1	5.0	W
	Write[2)]	4.3	5.4	W
	PS3[3)]	20	-	mW
	PS4[3)]	3	-	mW
2048GB	Read[2)]	4.1	5.7	W
	Write[2)]	4.4	5.4	W
	PS3[3)]	20	-	mW
	PS4[3)]	3	-	mW

Note:

1)Typical values reflect values obtained in specific test environments under typical test parameters. Actual results will vary based on the conditions and environment in which the part is used.

2)The values are specified at the condition causing maximum power consumption and PS0.

3)PS3 and PS4 are described in Sector 1.7 Power Mode Support. PCIe Link state is L1.2. Power consumption during the Admin command processing is excluded. This is Typical Power.

1.2.12. Temperature

Table 10 Temperature Relative Specifications[1)]

Environmental Class	Mode	Min	Max	Unit
Standard	Operating Temperature	0	85	°C
	Non-operating Temperature	-40	85	°C
	Humidity	5	95	%
Extended	Operating Temperature	-25	85	°C
	Non-operating Temperature	-40	85	°C
	Humidity	5	95	%
Industrial	Operating Temperature	-40	85	°C
	Non-operating Temperature	-40	85	°C
	Humidity	5	95	%

Note:

[1] Measured without condensation.

1.2.13. Reliability

Table 11 Reliability specifications

Parameter	Value
Mean Time to Failure (MTTF) [1]	> 3,000,000 hours
Power on/off cycle[2]	50,000 cycles

Notes:

[1] MTTF is calculated based on a Part Stress Analysis. It assumes nominal voltage with all other parameters within specified range.

[2] Power on/off cycles is defined as power being removed from the drive, and the restored. Most host systems remove power from the drive when entering suspend and hibernate as well as on a system shutdown.

1.2.14. Shock and Vibration

Table 12 Shock and Vibration

Item	Mode	Timing/Frequency	Max
Shock[1]	Operating Non-operating	At 0.5 msec half-sine	1500G
Vibration[2]	Operating Non-operation	10-2000 Hz	20 G Peak

Notes:

[1] Shock specifications assume that the SSD is mounted securely with the input vibration applied to the drive mounting screws. Stimulus may be applied in the X, Y or Z axis.

[2] Vibration specifications assume that the SSD is mounted securely with the input vibration applied to the drive mounting screws. Stimulus may be applied in the X, Y or Z axis. The measured specification is in root mean squared form.

1.2.15. Electrostatic discharge (ESD)

Electromagnetic Immunity tests assume the SSD is properly installed in the representative host system. The drive operates properly without errors degradation in performance when subjected to radio frequency (RF) environments defined in the following table.

Table 13 Radio Frequency Specifications

Test	Description	Performance criteria	Reference standard
Electrostatic discharge	Contact ±4KV Air: ±8KV	A	IEC 61000-4-2:2008
Electrostatic discharge	Contact ±6KV Air: ±12KV	B	IEC 61000-4-2:2008
Electrostatic discharge	Contact ±8KV Air: ±15KV	C	IEC 61000-4-2:2008
Radiated RF immunity	80~1000MHz, 3V/m, 80% AM with 1 KHz sine 900 MHz, 3 V/m, 50% pulse modulation at 200Hz	A	IEC 61000-4-3:2008
Electrical fast transient	±1KV on AC mains ±0.5KV on external I/O	B	IEC 61000-4-4:2004 +Corr.1:2006 +Corr.2:2007
Surge immunity	±1KV differential ±2KV common, AC mains	B	IEC 61000-4-5:2005
Conducted RF immunity	150KHz~80 MHz, 3 Vrms, 80% AM with 1KHz sine	A	IEC 61000-4-6:2008
Power frequency magnetic field	50Hz, 1A/m (r.m.s.)	A	IEC 61000-4-6:2008

Notes:

[1] Performance criterion A = The device shall continue to operate as intended, i.e., normal unit operation with no degradation of performance.

[2] Performance criterion B = The device shall continue to operate as intended after completion of test, however, during the test, some degradation of performance is allowed as long as there is no data loss operator intervention to restore device function.

[3] Performance criterion C = Temporary loss of function is allowed. Operator intervention is acceptable to restore device function.

[4] Contact electrostatic discharge is applied to drive enclosure.

1.2.16. Weight:

Weight spec. = 6.0g Max.（CL6-8D2048）

1.2.17. Dimension:

Form factor:

M.2 2230: 30.0 mm x 22.0 mm x 2.23 mm (L x W x H), 256GB – 1024GB

30.0 mm x 22.0 mm x 2.38 mm (L x W x H), 2048GB

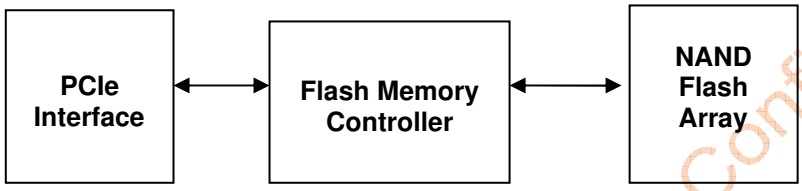
M.2 2242: 42.0 mm x 22.0 mm x 2.23 mm (L x W x H), 256GB – 1024GB

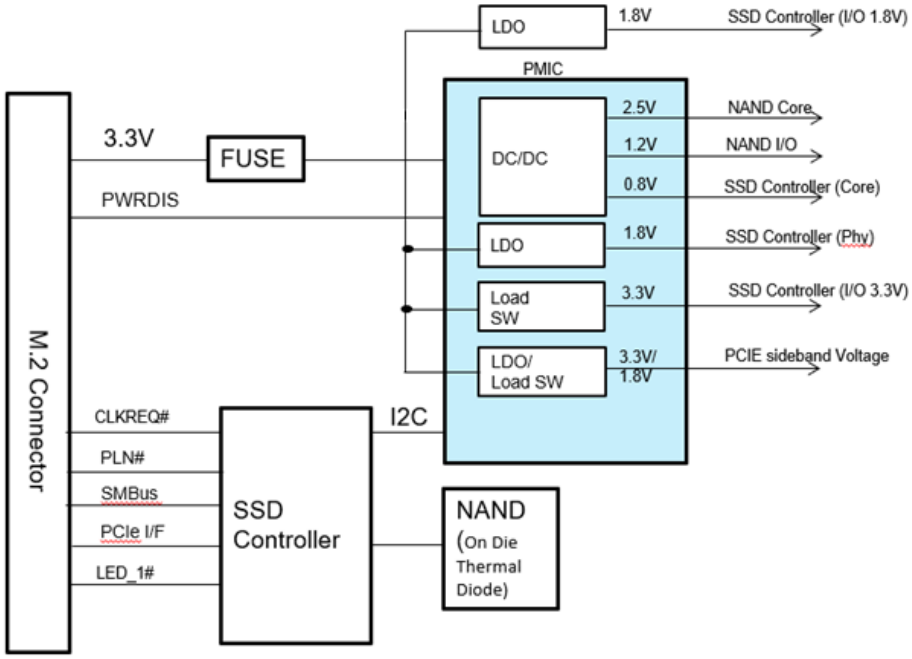
42.0 mm x 22.0 mm x 2.38 mm (L x W x H), 2048GB

M.2 2280: 80.0 mm x 22.0 mm x 2.23 mm (L x W x H), 256GB – 1024GB

80.0 mm x 22.0 mm x 2.38 mm (L x W x H), 2048GB

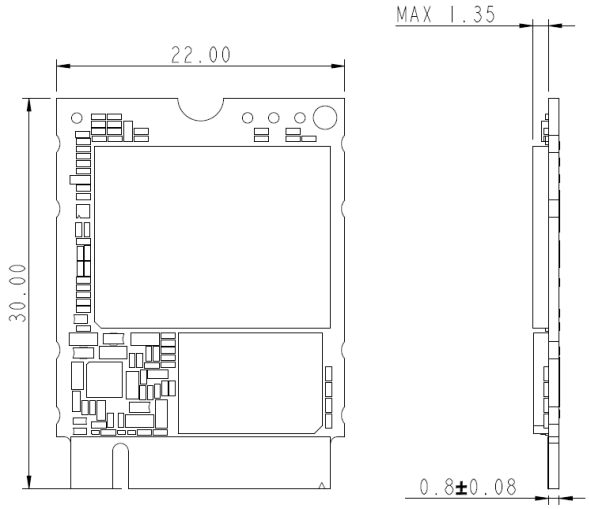
1.3 Functional Block Diagram



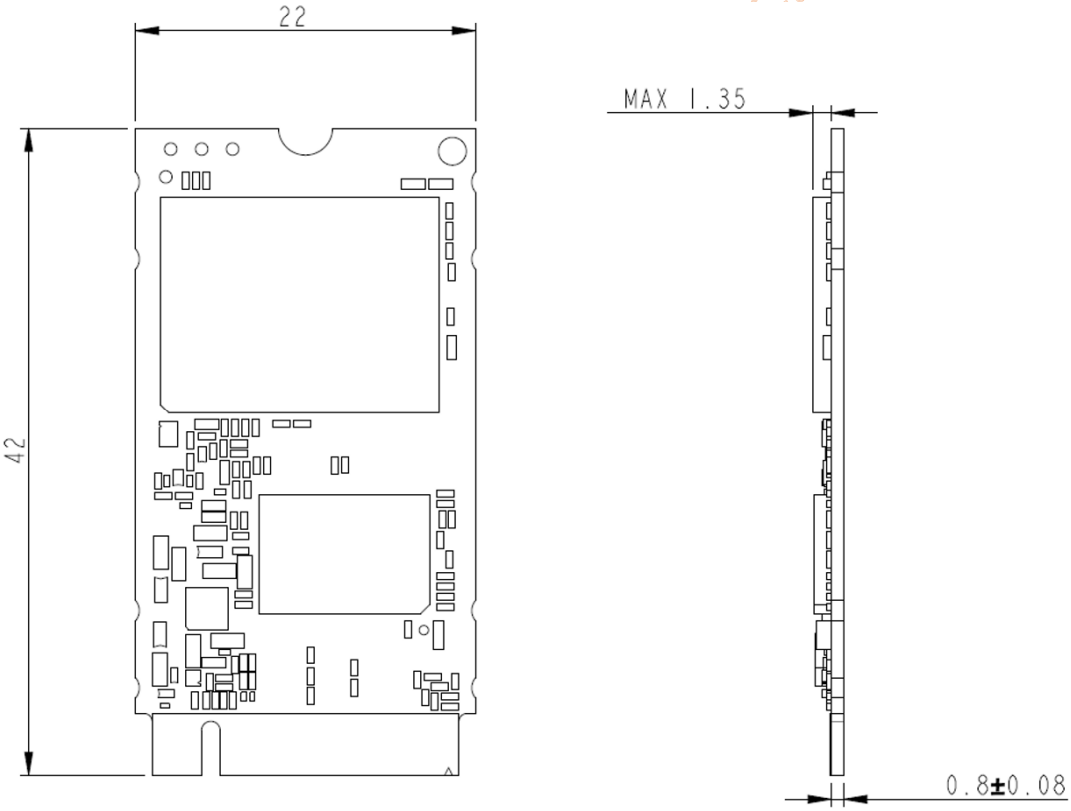


1.4 Mechanical Drawing:

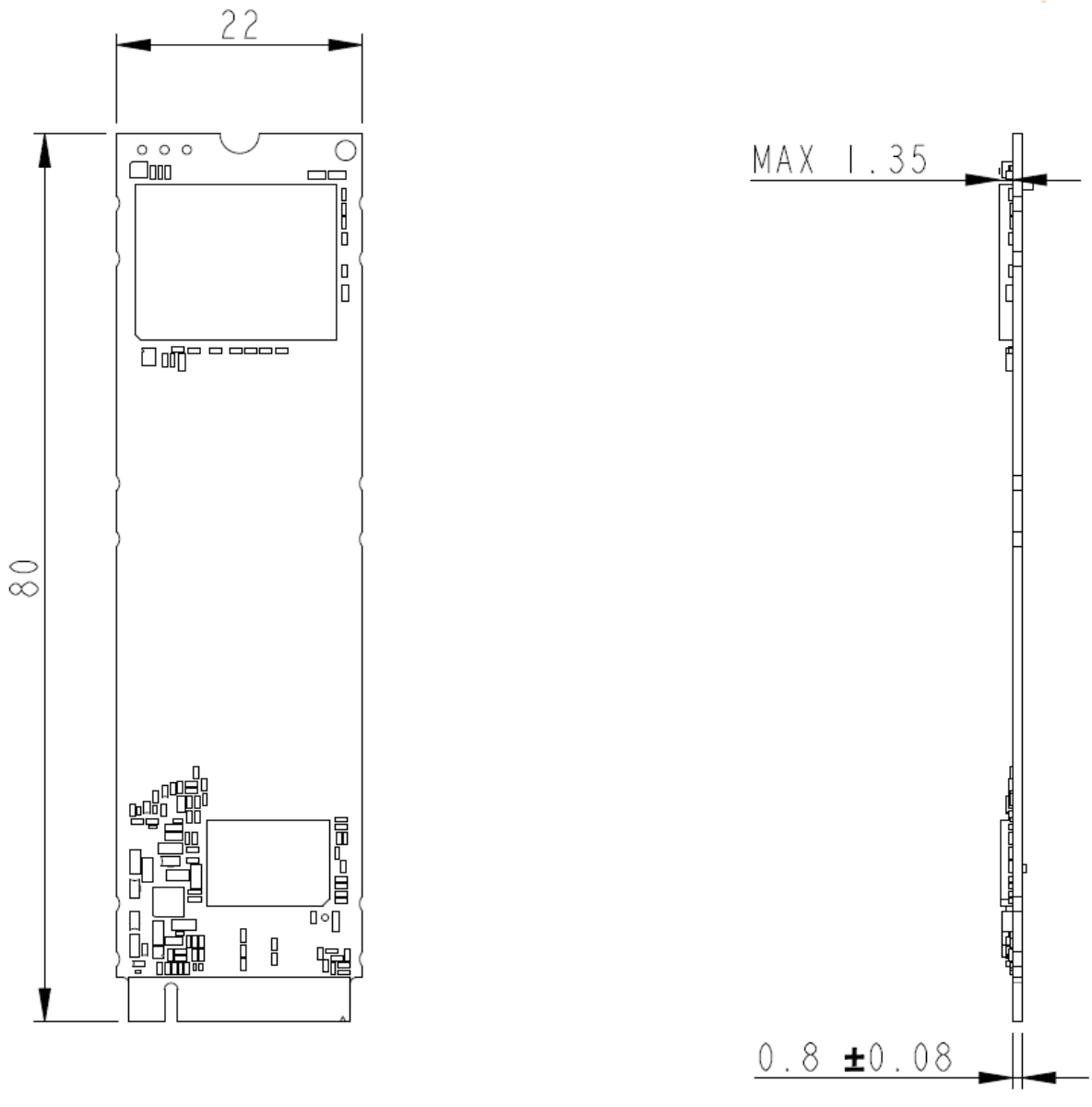
M.2 2230



M.2 2242



M.2 2280



1.5 Architecture

The CL6 PCIe Gen4 x 4 Lane Solid State Drive (SSD) utilizes a cost effective system-on-chip (SoC) design to provide a full 8GB/s bandwidth with the host while managing multiple flash memory devices on multiple channels internally.

1.6 Bootable Device:

The CL6 PCIe Gen4 x 4 Lane Solid State Drive (SSD) is configured as a bootable device. This supported function allows users to manage it as a main system drive and to boot from PCIe SSD.

1.7 Power Mode Support

PCI Express feature enables the hardware to engage actively in automatic Link power management.

CL6 PCIe Gen4 x 4 Lane SSD Supports L0, L1, L1.1 and L1.2 mode.

-L0: Full On (Active power / Active mode) @PS0

-L1: Idle (Lower power / Idle mode) @PS0

-L1.2: Sleep (Lower power / Sleep mode) @PS4

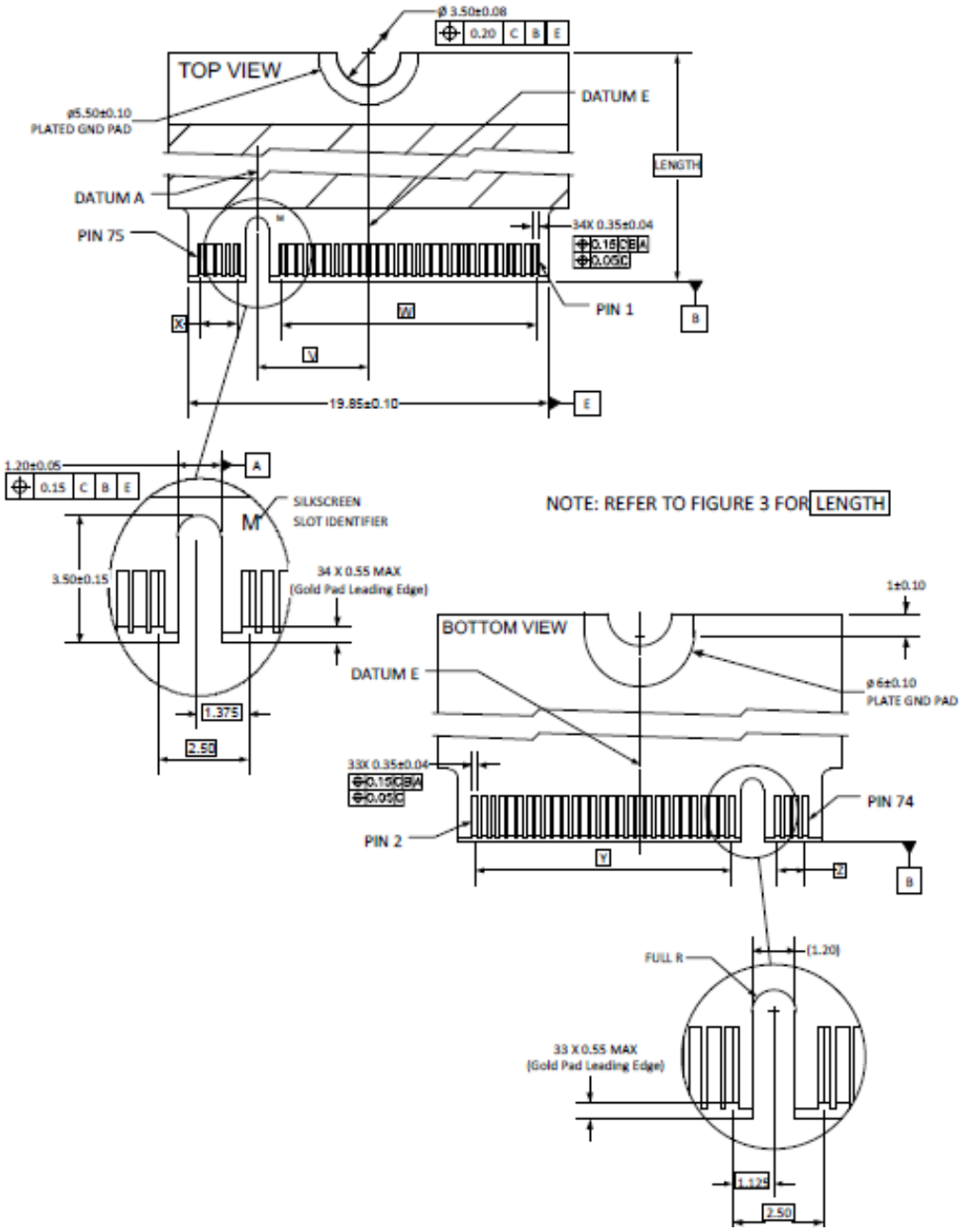
The Link state transits automatically from L0 to L1, L1.1, or L1.2 state to save power when there is no data transferring. The device reduces power by gating internal clocks, and the CLKREQ# signal transited by host will enable lower power mode of some internal components such as PCIe PHY. Once the data can be transferred across the Link, the state will be brought back to L0 by the hardware.

Input Voltage	**State**			**256 GB (W)**	**512 GB (W)**	**1024 GB (W)**	**2048 GB (W)**
3.3V ± 8%	PS0	Active Mode Max. Read/Write Performance (L0 state)	Rms	4.8	5.7	5.4	5.7
	PS3	Slumber Mode		0.02	0.02	0.02	0.02
	PS4	Sleep Mode (L1.2 state)		0.003	0.003	0.003	0.003

2 PIN LOCATIONS AND SIGNAL DESCRIPTIONS

2.1 Pin Locations

The data and power connector pin locations of the CL6 PCIe SSD Gen4 x 4 Lane are shown below. This M.2 device contains Socket 3 + M key.



2.2 M.2 Socket Definition

The PCI Express interface supported in Socket 3 is a 4 Lane PCI Express interface intended for premium SSD devices that need this sort of host interface.

	Soldered-down			Connectorized			
	Type	Module Height Options	Pinout Key	Connector Key	Type	Module Height Options	Module Key
Socket 1 Connectivity	1216	S1, S3	E	N/A	N/A	N/A	N/A
	N/A	N/A	N/A	A, E	1630	S1, D1, S3, D3, D4	A, E, A+E
	2226	S1, S3	E	A, E	2230	S1, D1, S3, D3, D4	A, E, A+E
	3026	S1, S3	A+E	A, E	3030	S1, D1, S3, D3, D4	A, E, A+E
Socket 2 WWAN/Other	N/A	N/A	N/A	B	3042	S1, D1, S3, D3, D4	B
Socket 2 SSD/Other	N/A	N/A	N/A	B	2230	S2, D2, S3, D3, D5	B+M
	N/A	N/A	N/A	B	2242	S2, D2, S3, D3, D5	B+M
	N/A	N/A	N/A	B	2260	S2, D2, S3, D3, D5	B+M
	N/A	N/A	N/A	B	2280	S2, D2, S3, D3, D5	B+M
	N/A	N/A	N/A	B	22110	S2, D2, S3, D3, D5	B+M
Socket 3 SSD Drive	N/A	N/A	N/A	M	2242	S2, D2, S3, D3, D5	M, B+M
	N/A	N/A	N/A	M	2260	S2, D2, S3, D3, D5	M, B+M
	N/A	N/A	N/A	M	2280	S2, D2, S3, D3, D5	M, B+M
	N/A	N/A	N/A	M	22110	S2, D2, S3, D3, D5	M, B+M

2.3 Socket 3 PCIe-based SSD Module Pinout

Pin #	Name	Description	Pin #	Name	Description
1	CONFIG_3	GND	2	+3.3V	3.3 V Source
3	GND	GND	4	+3.3V	3.3 V Source
5	PETn3	PCIe 3 Device Transmitter	6	PWRDIS	Power Disable
7	PETp3		8	PLN#	Power Loss Notification
9	GND	GND	10	LED1#	Device Activity
11	PERn3	PCIe 3 Device Receiver	12	+3.3V	3.3 V Source
13	PERp3		14	+3.3V	3.3 V Source
15	GND	GND	16	+3.3V	3.3 V Source
17	PETn2	PCIe 2 Device Transmitter	18	+3.3V	3.3 V Source
19	PETp2		20	Reserved	NC
21	GND	GND	22	VIO 1.8V	VIO 1.8V[1)]
23	PERn2	PCIe 2 Device Receiver	24	Reserved	NC
25	PERp2		26	Reserved	NC
27	GND	GND	28	Reserved	NC
29	PETn1	PCIe 1 Device Transmitter	30	Reserved	NC
31	PETp1		32	Reserved	NC
33	GND	GND	34	Reserved	NC
35	PERn1	PCIe 1 Device Receiver	36	Reserved	NC
37	PERp1		38	Reserved	NC
39	GND	GND	40	SMB_CLK	SMBus Clock
41	PETn0	PCIe 0 Device Transmitter	42	SMB_DATA	SMBus Data
43	PETp0		44	ALERT#	Alert
45	GND	GND	46	Reserved	NC
47	PERn0	PCIe 0 Device Receiver	48	Reserved	NC
49	PERp0		50	PERST#	PE-Reset
51	GND	GND	52	CLKREQ#	Clock Request
53	REFCLKn	PCIe Reference Clock	54	PEWAKE#	NC
55	REFCLKp		56	MFG_DATA	Manufacturing pin. Must be non-connect on the host board.
57	GND	GND	58	MFG_CLOCK	
Notch			Notch		
67	Reserved	NC	68	SUSCLK	NC
69	PEDET	OPEN	70	+3.3V	3.3 V Source
71	GND	GND	72	+3.3V	3.3 V Source
73	VIO_CFG	NC	74	+3.3V	3.3 V Source
75	GND	GND			

3 PCI EXPRESS

3.1 Interface

The PCI Express interface supports the x1 PCI Express interface (one Lane). A Lane consists of an input and an output high-speed differential pair. Also supported is a PCI Express reference clock. Refer to the PCI Express Base Specification for more details on the functional requirements for the PCI Express interface signals.

Socket 1 pin out has provisions for an additional PCI Express lane indicated by the suffix 1 to the signal names. These additional PETx1 and PERx1 signal sets can serve as the second Lane to the original PCI Express interface, or alternatively, they can be complimented with a second set of REFCLKx1 and a set of Auxiliary Signals on the adjacent reserved pins to form a complete second PCI Express x1 interface.

3.2 Auxiliary Signals

The auxiliary signals are provided on the system connector to assist with certain system level functionality or implementation. These signals are not required by the PCI Express architecture, but may be required by specific implementations such as PCI Express M.2 Card. The high-speed signal voltage levels are compatible with advanced silicon processes. The optional low speed signals are defined to use the +3.3V supply, as it is the lowest common voltage available. Most ASIC processes have high voltage (thick gate oxide) I/O transistors compatible with +3.3V. The use of the +3.3V supply allows PCI Express signaling to be used with existing control bus structures, avoiding a buffered set of signals and bridges between the buses.

The PCI Express M.2 Card add-in card and system connectors support the auxiliary signals that are described in the following sections.

3.3 Reference Clock

The REFCLK+/REFCLK- signals are used to assist the synchronization of the card's PCI Express interface timing circuits. Availability of the reference clock at the card interface may be gated by the CLKREQ# signal as described in section 3.1.5.1, CLKREQ# Signal. When the reference clock is not available, it will be in the parked state. A parked state is when the clock is not being driven by a clock driver and both REFCLK+ and REFCLK- are pulled to ground by the ground termination resistors. Refer to the PCI Express Card Electromechanical Specification for more details on the functional and tolerance requirements for the reference clock signals.

3.3.1 CLKREQ# Signal

The CLKREQ# signal is an open drain, active low signal that is driven low by the PCI Express M.2 add-I Card function to request that the PCI Express reference clock be available (active clock state) in order to allow the PCI Express interface to send/receive data. Operation of the CLKREQ# signal is determined by the state of the Enable Clock Power Management bit in the Link Control Register (offset 010h). When disabled, the CLKREQ# signal shall be asserted at all times whenever power is applied to the card, with the exception that it may be de-asserted during L1 PM Sub states. When enabled, the CLKREQ# signal may be de-asserted during the L1 Link state.

The CLKREQ# signal is also used by the L1 PM Sub states mechanism. In this case, CLKREQ# can be asserted by either the system or add-in card to initiate an L1 exit. See the PCI Express Base Specification for details on the functional requirements for the CLKREQ# signal when implementing L1 PM Sub states.

Whenever dynamic clock management is enabled and when a card stops driving CLKREQ# low, it indicates that the device is ready for the reference clock to transition from the active clock state to a parked (not available) clock state. Reference clocks are not guaranteed to be parked by the host system when CLKREQ# gets de-asserted and module designs shall be tolerant of an active reference clock even when CLKREQ# is de-asserted by the module.

The card must drive the CLKREQ# signal low during power up, whenever it is reset, and whenever it requires the reference clock to be in the active clock state. Whenever PERST# is asserted, including when the device is not in D0, CLKREQ# shall be asserted.

It is important to note that the PCI Express device must delay de-assertion of its CLKREQ# signal until it is ready for its reference clock to be parked. The device must be able to assert its clock request signal, whether or not the reference clock is active or parked, when it needs to put its Link back into the L0 Link state. Finally, the device must be able to sense an electrical idle break on its up-stream-directed receive port and assert its clock request, whether or not the reference clock is active or parked.

The assertion and de-assertion of CLKREQ# are asynchronous with respect to the reference clock. Add-in cards that do not implement a PCI Express interface shall leave this output unconnected on the card. CLKREQ# has additional electrical requirements over and above standard open drain signals that allow it to be shared between devices that are powered off and other devices that may be powered on. The additional requirements include careful circuit design to ensure that a voltage applied to the CLKREQ# signal network never causes damage to a component even if that particular component's power is not applied.

Additionally, the device must ensure that it does not pull CLKREQ# low unless CLKREQ# is being intentionally asserted in all cases; including when the related function is in D3cold. This means that any component implementing CLKREQ# must be designed such that:

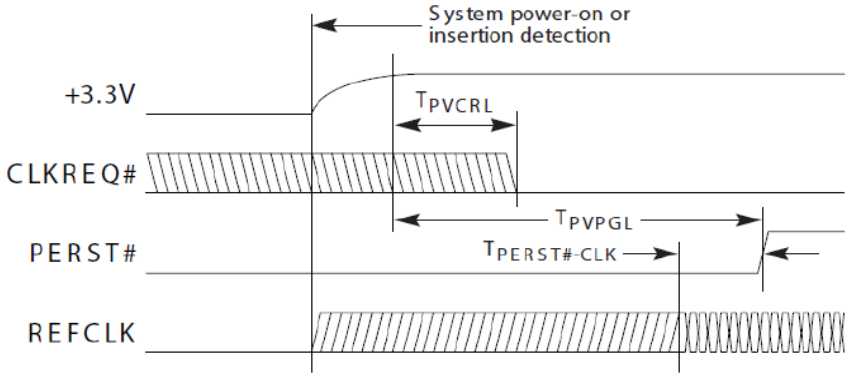
-Unpowered CLKREQ# output circuits are not damaged if a voltage is applied to them from other powered "wire-Red" sources of CLKREQ#.

-When power is removed from its CLKREQ# generation logic, the unpowered output does not present a low impedance path to ground or any other voltage.

These additional requirements ensure that the CLKREQ# signal network continues to function properly when a mixture of powered and unpowered components have their CLKREQ# outputs wire-ORed together. It is important to note that most commonly available open drain and tri-state buffer circuit designs used "as is" do not satisfy the additional circuit design requirements for CLKREQ#.

3.3.2 Power-up Requirements

CLKREQ# is asserted in response to PERST# assertion. On power up, CLKREQ# must be asserted by a PCI Express device within a delay (TPVCRL) from the power rails achieving specified operating limits and PERST# assertion (see below Figure). This delay is to allow adequate time for the power to stabilize on the card and certain system functions to start prior to the card starting up. CLKREQ# may not be de-asserted while PERST# is asserted.



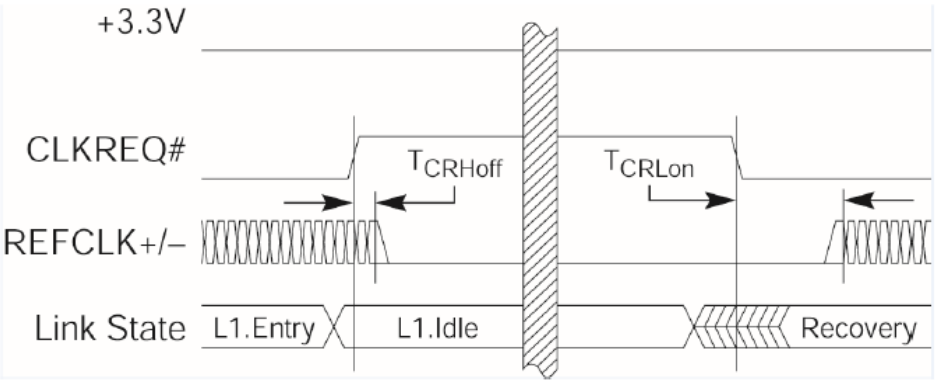
Note: T_{PVCRL} is measured from the later rising edge of +3.3V.

3.3.3 Dynamic Clock Control

After a PCI Express device has powered up and whenever its upstream link enters the L1 link state, it shall allow its reference clock to be turned off (put into the parked clock state). To accomplish this, the device de-asserts CLKREQ# (high) and must allow that the reference clock will transition to the parked clock state within a delay (TCRHoff). Figure 79 shows the CLKREQ# clock control timing diagram.

To exit L1, the device must assert CLKREQ# (low) to re-enable the reference clock. After the device asserts CLKREQ# (low) it must allow that the reference clock will continue to be in the parked clock state for a delay (TCRLon) before transitioning to the active clock state. The time that it takes for the device to assert CLKREQ# and for the system to return the reference clock to the active clock state are serialized with respect to the remainder of L1 recovery. This time must be taken into account when the device is reporting its L1 exit latency.

When the PCI Express device supports, and is enabled for, Latency Tolerance Reporting (LTR), the device must allow that the reference clock transition to the active clock state may be additionally delayed by the system up to a maximum value consistent with requirements for the LTR mechanism. During this delay, the reference clock must remain parked. When exiting the parked state following the delay, the clock must be stable and valid within 400 ns.



3.3.4 Clock Request Support Reporting and Enabling

Support for the CLKREQ# dynamic clock protocol should be reported using bit 18 in the PCI Express link capabilities register (offset 0C4h). To enable dynamic clock management, bit 8 of the Link Control register (offset 010h) is provided. By default, the card shall enable CLKREQ# dynamic clock protocol upon initial power up and in response to any warm reset by the host system. System software may subsequently disable this feature as needed. Refer to the PCI Express Base Specification, Revision 1.1 (or later) for more information regarding these bits.

3.3.5 PERST# Signal

-The PERST# signal is de-asserted to indicate when the system power sources are within their specified voltage tolerance and are stable.

-PERST# should be used to initialize the card functions once power sources stabilize.

-PERST# is asserted when power is switched off and also can be used by the system to force a hardware reset on the card.

-System may use PERST# to cause a warm reset of the add-in card.

Refer to the PCI Express Card Electromechanical Specification for more details on the functional requirements for the PERST# signal.

4 ADMIN COMMAND SETS

4.1 Admin Command

The CL6 PCIe Gen4 x 4 Lane SSD supports all the mandatory Admin commands defined in the NVMe 1.4 specification which consists of

- Delete I/O Submission Queue
- Create I/O Submission Queue
- Get Log Page
- Delete I/O Completion Queue
- Create I/O Completion Queue
- Identify
- Abort
- Set Features
- Get Features
- Asynchronous Event Request

The CL6 PCIe Gen4 x 4 Lane SSD supports all the following optional commands

- Firmware Commit
- Firmware Image Download
- Security Send
- Security Receive
- Device Self-test
- Format NVM
- Sanitize

4.2 Namespace Feature Set

CL6 without support this feature set.

4.3 Security Feature Set

The Security Receive command transfers the status and data result of one or more Security Send commands that were previously submitted to the controller.

The association between a Security Receive command and previous Security Send commands is dependent on the Security Protocol. The format of the data to be transferred is dependent on the Security Protocol. Refer to SPC-4 for Security Protocol details.

Each Security Receive command returns the appropriate data corresponding to a Security Send command as defined by the rules of the Security Protocol. The Security Receive command data may not be retained if there is a loss of communication between the controller and host, or if a controller reset occurs.

The Security Send command is used to transfer security protocol data to the controller. The data structure transferred to the controller as part of this command contains security protocol specific commands to be performed by the controller. The data structure transferred may also contain data or parameters associated with the security protocol commands. Status and data that is to be returned to the host for the security protocol commands submitted by a Security Send command are retrieved with the Security Receive command.

5 NVME COMMAND SETS

5.1 NVMe Command

The CL6 PCIe Gen4 x 4 Lane SSD supports all the mandatory NVMe commands defined in the NVMe 1.4 specification, which consists of

- Flush
- Write
- Read

The CL6 PCIe Gen4 x 4 Lane SSD supports all the following optional commands

- Write Uncorrectable
- Dataset Management
- Write Zeroes
- Verify

5.2 Power Management Feature Set

The power management capability allows the host to manage NVM subsystem power statically or dynamically. Static power management consists of the host determining the maximum power that may be allocated to an NVM subsystem and setting the NVM Express power state to one that consumes this amount of power or less. Dynamic power management consists of the host modifying the NVM Express power state to best satisfy changing power and performance objectives. This power management mechanism is meant to complement and not replace autonomous power management performed by a controller.

Associated with each power state is a Power State Descriptor in the Identify Controller data structure. The descriptors for all implemented power states may be viewed as forming a table as shown for a controller with three implemented power states. The Maximum Power (MP) field indicates the instantaneous maximum power that may be consumed in that state. The controller may employ autonomous power management techniques to reduce power consumption below this level, but under no circumstances is power allowed to exceed this level.

5.3 Host Memory Buffer

The Host Memory Buffer feature allows the controller to utilize an assigned portion of host memory exclusively. The use of the host memory resources is vendor specific. Host software may not be able to provide any or a limited amount of the host memory resources requested by the controller. The controller shall function properly without host memory resources.

During initialization, host software may provide a descriptor list that describes a set of host memory address ranges for exclusive use by the controller. The host memory resources assigned are for the exclusive use of the controller (host software should not modify the ranges) until host software requests that the controller release the ranges and the controller completes the Set Features command. The controller is responsible for initializing the host memory resources. Host software should request that the controller release the assigned ranges prior to a shutdown event, a Runtime D3 event, or any other event that requires host software to reclaim the assigned ranges. After the controller acknowledges that it is no longer using the ranges, host software may reclaim the host memory resources. In the case of Runtime D3, host software should provide the host memory resources to the controller again and inform the controller that the ranges were in use prior to the RTD3 event and have not been modified.

The host memory resources are not persistent in the controller across a reset event. Host software should provide the previously allocated host memory resources to the controller after the reset completes. If host software is providing previously allocated host memory resources (with the same contents) to the controller, the Memory Return bit is set to '1' in the Set Features command.

The controller shall ensure that there is no data loss or data corruption in the event of a surprise removal while the Host Memory Buffer feature is being utilized.

6 REFERENCES

This document references standards defined by a variety of organizations as listed below.

Table 65 Standards References

Title	Location
VCCI	http://www.vcci.or.jp/vcci_e/general/join/index.html
ROHS	Search for material description datasheet at http://intel.pcnalert.com
SFF-8144, 1.8” drive form factor	http://www.sffcommittee.org
PCI Express Specification	http://www.pcisig.com
SFF-8223, 2.5” Drive w/Serial Attachment Connector	http://www.sffcommittee.org
SFF-8201, 2.5” drive form factor	http://www.sffcommittee.org
NVM Express Specification	http://www.nvmexpress.org
International Electro Technical Commission EB61000 4-2 Personnel Electrostatic Discharge Immunity 4-3 Electromagnetic compatibility (EMC) 4-4 Electromagnetic compatibility (EMC) 4-5 Electromagnetic compatibility (EMC) 4-6Electromagnetic compatibility (EMC) 4-11 (Voltage variations)	http://www.iec.ch
ENV 50204 (Radiated electromagnetic field from digital radio telephones)	http://www.iec.ch

7 TERMS AND ACRONYMS

This document incorporates many industry- and device-specific words use the following list to define a variety of terms and acronyms.

Table 76 Glossary of Terms and Acronyms

Term	Definition
BER	Bit Error Rate, or percentage of bits that have errors relative to the total number of bits received
BIOS	Basic Input/Output System
Chipset	A term used to define a collection of integrated components required to make a PC function
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
EXT	Extended
FP	First Party
GB	Giga-byte defined as $1X10^9$ bytes
HCI	Host Controller Interface
HCT	Hardware Compatibility Test
HDD	Hard Disk Drive
IOPS	Input output operations per second
LBA	Logical Block Address
MB	Mega-bytes defined as $1x10^6$ bytes
mSATA	Mini-SATA
MTTF	Mean time to failure
NCQ	Native Command Queuing The ability of the SATA hard drive to re-order commands in order to maximize the efficiency of gathering data from the platters
NOP	No operation
NTFS	NT file system
OEM	Original Equipment Manufacturer
OS	Operation System
Port	The point at which a SATA drive physically connected to the SATA controller
RAID	Redundant Array of Independent Disks
RMS	Root Mean Squared
RPM	Revolutions per Minute
RTM	Release to Manufacture
SATA	Serial ATA
SFF	Small Form Factor
SMART	Self-Monitoring, Analysis and reporting Technology An open standard for developing hard drive and software systems that automatically monitors a hard drive's health and reports potential problems

SSD	Solid State Drive
TBD	To Be Determined
WHQL	Microsoft* Windows Hardware Quality Labs
Write Cache	A memory device within a hard drive, which is allocated for the temporary storage of data before that data is copied to its permanent storage location
VCCI	Voluntary Control Council for Interface
A	Amperage or Amp
DC	Direct Current
GND	Ground
GNSS	Global Navigation Satellite System (GPS+GLONASS)
HDR	Hybrid Digital Radio
HSIC	High Speed Inter-Chip
I/F	Interface
I/O	Input/Output
IR	Current x Resistance = Voltage
I2C	Inter-Integrated Circuit
I2S	Integrated Interchip Sound
LED	Light Emitting Diode
LGA	Laned Grid Array
mΩ	milli Ohm
mA	milli Amp
mV	milli Volt
NFC	Near Field Communications
M.2	Formally called Next Generation Form Factor (NGFF)
NB	Notebook
NIC	Network Interface Card
NC	Not Connected
SATA	Serial Advanced Technology Attachment or Serial ATA
PCIe	Peripheral Component Interconnect Express
PCM	Pulse Code Modulation
SDIO	Secure Digital Input Output
SIM	Subscriber Identity Module
SSD	Sold-State Storage Device
RF	Radio Frequency
RM	Root Mean Square
RoHS	Restriction of Hazardous Substances Directive
RTC	Real Time Clock
RFU	Reserved for Future Use
UIM	User Identity Module
UART	Universal Asynchronous Receive Transmit
W	Wattage or Watts
WiGig	Wireless Giga communication
WLANE	Wireless Local Area Network
WPAN	Wireless Personal Area Network
WWAN	Wireless Wide Area Network

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